CACHE COHERENCE PROTOCOLS ANALYZER

A tool for analyzing how different Snooping based Cache Coherence Protocols perform under varying workloads

15-618 SPRING 2017 FINAL PROJECT

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WHAT DID WE MAKE?

▸ Cache Simulator
  ▸ Generate memory traces
  ▸ Analyze the memory traces
    ▸ Multiple snooping based cache protocol
    ▸ Mimic real world system behavior
WHAT ARE WE TRYING TO SOLVE?

- Have a problem to solve
- Need to design a system to solve it
- What kind of cache coherence protocol can we use?
- Our tool will help you decide!
SYSTEM DESIGN

CPU 1
CACHE

CPU 2
CACHE

CPU 3
CACHE

CPU 4
CACHE

Response Bus (Snooping)
Request Bus (Memory Tx)

Request Table
Memory

PROTOCOLS

- Write Invalidate Protocols
- MSI
- MESI
- MOESI
- Write-Update Protocol
- Dragon
- Hybrid Protocol
- Competitive Snooping (!)
HOW DO WE COMPARE THE PROTOCOLS?

- Number of Bus Transactions
- Number of Memory Requests
- Number of Memory Write-Backs
- Number of Cache to Cache Transfers
HOW DO WE GENERATE THE MEMORY TRACE?

- Intel Pin-tool
- Memory trace of a program
- Problem?
  - Relevance of functions
  - HUGE!
- Solution
  - Dummy functions
WHAT DID THE TOOL HELP US ANALYZE?
BENEFIT OF ‘E’ STATE

BUS Tx vs MEM Reqs vs MEM WriteBacks (MSI vs Mesi)

Mandelbrot (5mb Trace)
BENEFIT OF ‘O’ STATE

BUS Tx, MEM Reqs vs MEM WriteBacks (MSI v MOSI)

Wild Fill Bucket

BENEFIT OF ‘O’ STATE
WRITE INVALIDATE vs WRITE UPDATE

BUS Tx, MEM WB and CACHE Tran (MOESI v Dragon)

Pagerank (tiny graph)
COMPETITIVE SNOOPING (!)

OCEAN: p=4, n=18

BFS - top_down - 100x100 grid
WHICH ONE WOULD YOU CHOOSE?
THANK YOU!

Kshitiz Dange and Yash Tibrewal
MSI Protocol

M (Modified)

PrRd / BusRdX

PrWr / BusRdX

S (Shared)

PrRd / --
BusRd / --

I (Invalid)

PrRd / BusRd

BusRdX / flush

BusRdX / flush
M (Modified)

O (Owner)

I (Invalid)

S (Shared)

PrWr / BusUpgr

BusRd / flush

PrRd / --

PrRd / --

BusRdX / --

BusUpgr / --

PrWr / BusUpgr

MOSI Protocol

BusRd / --

BusRdX / --

BusUpgr / --

PrRd / BusRd

PrRd / --

BusRd / flush

BusRd / flush
MOESI Protocol

M (Modified)
- PrRd / BusUpgr
- PrWr / --

O (Owner)
- PrRd / BusRd / flush
- BusRd / flush

I (Invalid)
- PrWR / BusRdX

E (Exclusive)
- PrRd / BusRd
- PrUpgr / BusUpgr
- BusRdX / flush
- BusUpgr / --

S (Shared)
- PrRd / BusRd
- BusRd / flush
You can:

- Specify the Number of Cores
- Specify the cache size
- Specify the associativity of cache
- Specify the program trace to analyze
- Specify the snooping protocol to use